

M5M44400AWJ, J, L, TP, RT-6, -7, -8, -6L, -7L, -8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

The M5M44400ATP, RT are packaged in a 26-pin very thin and small outline package which is a high reliability and high density surface mount device. Two types of devices are available. M5M44400ATP (normal lead bend type package), M5M44400ART (reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

Stand-by current is small enough for battery back-up application (L version).

FEATURES

Type name	RAS access time (max ns)	CAS access time (max ns)	Address access time (max ns)	OE access time (max ns)	Cycle time (min ns)	Power dissipation (typ mW)
M5M44400AXX-6, -6L	60	15	30	15	120	400
M5M44400AXX-7, -7L	70	20	35	20	140	350
M5M44400AXX-8, -8L	80	20	40	20	160	300

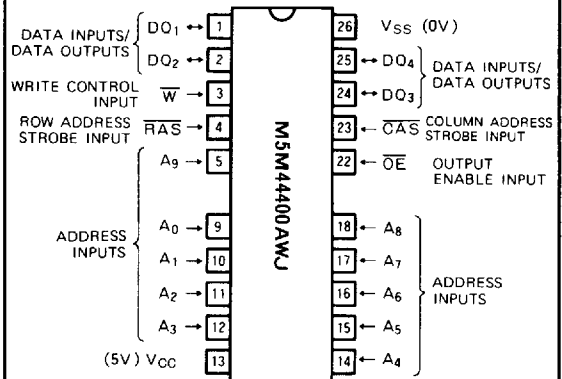
XX=WJ, J, L, TP, RT

- Standard 26 pin SOJ, 20 pin ZIP, 26 pin TSOP
- Single 5V ± 10% supply
- Low stand-by power dissipation
 - M5M44400AWJ, J, L, TP, RT 5.5mW (max)
 - M5M44400AWJ, J, L (L) 1.10mW (max)
 - M5M44400ATP, RT (L) 1.65mW (max)
- Low operating power dissipation
 - M5M44400Axx-6, -6L 550.0mW (max)
 - M5M44400Axx-7, -7L 467.5mW (max)
 - M5M44400Axx-8, -8L 412.5mW (max)
- Fast-page mode (1024-bit random access), Read-modify-write, RAS-only refresh, CAS before RAS refresh, Hidden refresh capabilities
- Early write operation and OE to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms / 128ms (L) (A₀ ~ A₉)
- 16-bit parallel test mode capability

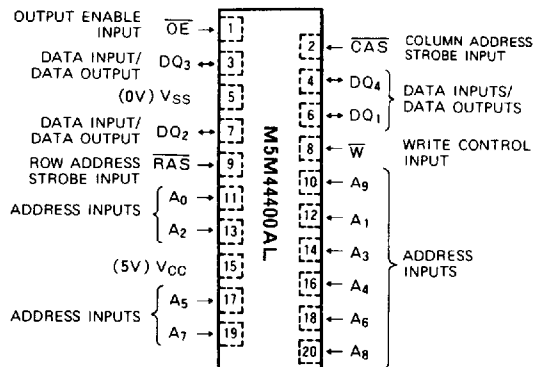
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



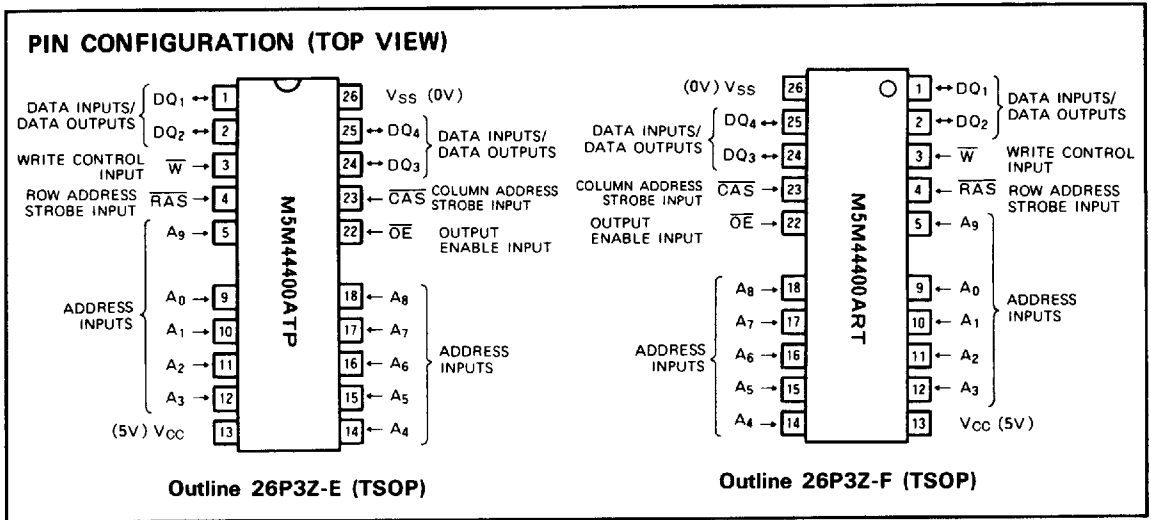
Outline 26P0Z (WJ:350 mil SOJ)
26P0J (J:300mil SOJ)



Outline 20P5L-B (ZIP)

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FUNCTION

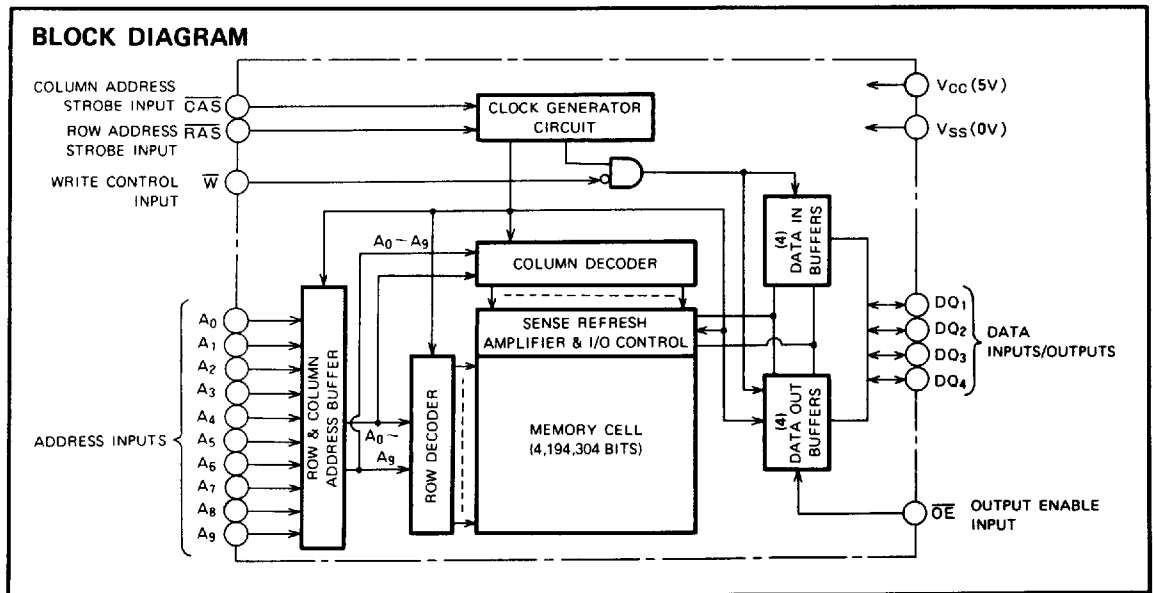
The M5M44400AWJ, J, L, TP, RT provide, in addition to normal read, write, and read-modify-write operations,

a number of other functions, e.g., fast page mode, $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT active, NAC nonactive, DNC don't care, VLD valid, IVD invalid, APD applied, OPN open



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1 ~ 7	V
V _I	Input voltage		-1 ~ 7	V
V _O	Output voltage		-1 ~ 7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a = 25°C	1000	mW
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.5	V
V _{IL}	Low level input voltage	DQ ₁ ~ DQ ₄	-1.0	0.8	V
		Others	-2.0	0.8	V

Note 1 All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	High-level output voltage	I _{OH} = -5mA	2.4		V _{CC}	V
V _{OL}	Low-level output Voltage	I _{OL} = 4.2mA	0		0.4	V
I _{OZ}	Off-state output current	Q floating 0V ≤ V _{OUT} ≤ 5.5V	-10		10	μA
I _I	Input current	0V ≤ V _{IN} ≤ 6.5, Other input pins = 0V	-10		10	μA
I _{CC1(AV)}	Average supply current from V _{CC} operating (Note 3, 4)	M5M44400A-6, -6L	R _{AS} , C _{AS} cycling		100	mA
		M5M44400A-7, -7L	t _{RC} = t _{WC} = min output open		85	
		M5M44400A-8, -8L			75	
I _{CC2(AV)}	Supply current from V _{CC} stand-by (Note 5)	M5M44400AWJ, J, L(L)	R _{AS} = C _{AS} = V _{IH} , output open		2	mA
		M5M44400ATP, RT(L)	R _{AS} = C _{AS} ≥ V _{CC} - 0.5V, output open		0.2	
					0.3	
I _{CC3(AV)}	Average supply current from V _{CC} refreshing (Note 3)	M5M44400A-6, -6L	R _{AS} cycling C _{AS} = V _{IH}		100	mA
		M5M44400A-7, -7L	t _{RC} = min. output open		85	
		M5M44400A-8, -8L			75	
I _{CC4(AV)}	Average supply current from V _{CC} Fast-Page-Mode (Note 3, 4)	M5M44400A-6, -6L	R _{AS} = V _{IL} , C _{AS} cyclin		100	mA
		M5M44400A-7, -7L	t _{PC} = min. output open		85	
		M5M44400A-8, -8L			75	
I _{CC6(AV)}	Average supply current from V _{CC} C _{AS} before R _{AS} refresh mode (Note 3)	M5M44400A-6, -6L	C _{AS} before R _{AS} refresh cycling		85	mA
		M5M44400A-7, -7L	t _{RC} = min output open		75	
		M5M44400A-8, -8L			65	
I _{CC8(AV)}	Average supply current from V _{CC} Battery back-up (Note 5)	M5M44400AWJ, J, L(L)	C _{AS} ≤ 0.2V or C _{AS} before R _{AS} refresh cycling W ≤ 0.2V (Except for RAS falling edge) or ≥ V _{CC} - 0.2V		0.2	mA
		M5M44400ATP, RT(L)	A ₀ ~ A ₁₀ ≤ 0.2V or ≥ V _{CC} - 0.2V D ≤ 0.2V or ≥ V _{CC} - 0.2V Q = open t _{RC} = 125μs t _{RAS} = t _{RASmin} ~ 1μs		0.3	

Note 2 Current flowing into an IC is positive, out is negative

3 I_{CC1(AV)}, I_{CC3(AV)} and I_{CC4(AV)} are dependent on cycle rate. Maximum current is measured at the fastest cycle rate

4 I_{CC1(AV)} and I_{CC4(AV)} are dependent on output loading. Specified values are obtained with the output open

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CAPACITANCE (Ta = 0 ~ 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Ci(A)	Input capacitance, address inputs	Vi = VSS f = 1MHz Vi = 25 mVrms			5	pF
	M5M44400AWJ, J, TP, RT				6	pF
	M5M44400AL				7	pF
Ci(OE)	Input capacitance, OE input				7	pF
Ci(W)	Input capacitance, write control input				7	pF
Ci(RAS)	Input capacitance, RAS input				7	pF
Ci(CAS)	Input capacitance, CAS input				7	pF
Ci/o	Input/Output capacitance, data ports			7	pF	

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted) (Notes 5, 12, 13)

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from CAS (Note 6, 7)		15		20		20	ns
tRAC	Access time from RAS (Note 6, 8)		60		70		80	ns
tAA	Column Address access time (Note 6, 9)		30		35		40	ns
tCPA	Access time from CAS precharge (Note 6, 10)		35		40		45	ns
tOEA	Access time from OE (Note 6)		15		20		20	ns
tOLZ	Output low impedance time from CAS low (Note 6)	5		5		5		ns
tOFF	Output disable time after CAS high (Note 11)	0	15	0	20	0	20	ns
tOEZ	Output disable time after OE high (Note 11)	0	15	0	20	0	20	ns

- Note 5 An initial pause of 500µs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS clock such as RAS-Only refresh)
 Note the RAS may be cycled during the initial pause. And any 8 RAS or RAS/CAS cycles are required after prolonged periods (greater than 16.4/128ms (L)) of RAS inactivity before proper device operation is achieved
- 6 Measured with a load circuit equivalent to 2TTL loads and 100pF
- 7 Assumes that tRCD ≥ tRCD(max) and tASC ≥ tASC(max)
- 8 Assumes that tRCD ≤ tRCD(max) and tRAD ≤ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD or tRAD exceeds the value shown
- 9 Assumes that tRAD ≥ tRAD(max) and tASC ≤ tASC(max)
- 10 Assumes that tCP ≤ tCP(max) and tASC ≥ tASC(max)
- 11 tOFF(max) and tOEZ(max) defines the time at which the output achieves the high impedance state (IOUT ≤ ±10µA) and is not reference to VOH(min) or VOL(max)

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TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

($T_a = 0 \sim 70^\circ C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Notes 12-13)

Symbol	Parameter	Limits						Unit	
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L			
		Min	Max	Min	Max	Min	Max		
t_{REF}	Refresh cycle time	M5M44400A		16.4		16.4		16.4	ms
		M5M44400A (L)		128		128		128	ns
t_{RP}	\overline{RAS} high pulse width	50		60		70		ns	
t_{RCD}	Delay time, \overline{RAS} low to \overline{CAS} low (Note 14)	20	45	20	50	20	60	ns	
t_{CRP}	Delay time, \overline{CAS} high to \overline{RAS} low	10		10		10		ns	
t_{RPC}	Delay time, \overline{RAS} high to \overline{CAS} low	0		0		0		ns	
t_{CPN}	\overline{CAS} high pulse width	10		10		10		ns	
t_{RAD}	Column address delay time from \overline{RAS} low (Note 15)	15	30	15	35	15	40	ns	
t_{ASR}	Row address setup time before \overline{RAS} low	0		0		0		ns	
t_{ASC}	Column address setup time before \overline{CAS} low (Note 16)	0	10	0	10	0	15	ns	
t_{RAH}	Row address hold time after \overline{RAS} low	10		10		10		ns	
t_{CAH}	Column address hold time after \overline{CAS} low	15		15		15		ns	
t_{DZC}	Delay time, data to \overline{CAS} low (Note 17)	0		0		0		ns	
t_{DZO}	Delay time, data to \overline{OE} low (Note 17)	0		0		0		ns	
t_{CDD}	Delay time, \overline{CAS} high to data (Note 18)	15		20		20		ns	
t_{ODD}	Delay time, \overline{OE} high to data (Note 18)	15		20		20		ns	
t_T	Transition time (Note 19)	1	50	1	50	1	50	ns	

- Note 12 The timing requirements are assumed $t_T = 5ns$
- 13 $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals
- 14 $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC} . If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA} . $t_{RCD(min)}$ is specified as $t_{RAH(min)} + 2t_T + t_{ASC(min)}$
- 15 $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}
- 16 $t_{ASC(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}
- 17 Either t_{DZC} or t_{DZO} must be satisfied
- 18 Either t_{CDD} or t_{ODD} must be satisfied
- 19 t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	120		140		160		ns
t_{RAS}	\overline{RAS} low pulse width	60	10000	70	10000	80	10000	ns
t_{CAS}	\overline{CAS} low pulse width	15	10000	20	10000	20	10000	ns
t_{CSH}	\overline{CAS} hold time after \overline{RAS} low	60		70		80		ns
t_{RSH}	\overline{RAS} hold time after \overline{CAS} low	15		20		20		ns
t_{RCS}	Read setup time before \overline{CAS} low	0		0		0		ns
t_{RCH}	Read hold time after \overline{CAS} high (Note 20)	0		0		0		ns
t_{RRH}	Read hold time after \overline{RAS} high (Note 20)	10		10		10		ns
t_{RAL}	Column address to \overline{RAS} hold time	30		35		40		ns
t_{OCH}	\overline{CAS} hold time after \overline{OE} low	15		20		20		ns
t_{ORH}	\overline{RAS} hold time after \overline{OE} low	15		20		20		ns

Note 20. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle

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Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t _{WC}	Write cycle time	120		140		160		ns
t _{RAS}	RAS low pulse width	60	10000	70	10000	80	10000	ns
t _{CAS}	CAS low pulse width	15	10000	20	10000	20	10000	ns
t _{CSH}	CAS hold time after RAS low	60		70		80		ns
t _{RSH}	RAS hold time after CAS low	15		20		20		ns
t _{WCS}	Write setup time before CAS low (Note 22)	0		0		0		ns
t _{WCH}	Write hold time after CAS low	10		15		15		ns
t _{CWL}	CAS hold time after W low	15		20		20		ns
t _{RWL}	RAS hold time after W low	15		20		20		ns
t _{WP}	Write pulse width	10		15		15		ns
t _{DS}	Data setup time before CAS low or W low	0		0		0		ns
t _{DH}	Data hold time after CAS low or W low	10		15		15		ns
t _{OEH}	OE hold time after W low	15		20		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t _{RWC}	Read write/read modify write cycle time (Note 21)	160		185		205		ns
t _{RAS}	RAS low pulse width	95	10000	115	10000	125	10000	ns
t _{CAS}	CAS low pulse width	50	10000	65	10000	65	10000	ns
t _{CSH}	CAS hold time after RAS low	95		115		125		ns
t _{RSH}	RAS hold time after CAS low	50		65		65		ns
t _{RCS}	Read setup time before CAS low	0		0		0		ns
t _{CWD}	Delay time, CAS low to W low (Note 22)	35		40		40		ns
t _{RWD}	Delay time, RAS low to W low (Note 22)	80		90		100		ns
t _{AWD}	Delay time address to W low (Note 22)	50		55		60		ns
t _{CWL}	CAS hold time after W low	15		20		20		ns
t _{RWL}	RAS hold time after W low	15		20		20		ns
t _{WP}	Write pulse width	10		15		15		ns
t _{DS}	Data setup time before W low	0		0		0		ns
t _{DH}	Data hold time after W low	10		15		15		ns
t _{OEH}	OE hold time after W low	15		15		20		ns

Note 21 t_{RWC} is specified as t_{RWC(min)} = t_{RAC(max)} + t_{O_D(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_t
 Note 22 t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are specified as reference points only. If t_{WCS} ≥ t_{WCS(min)} the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If t_{CWD} ≥ t_{CWD(min)}, t_{RWD} ≥ t_{RWD(min)}, t_{AWD} ≥ t_{AWD(min)} and t_{CPWD} ≥ t_{CPWD(min)} (for fast page mode cycle only), the cycle is a read modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to V_{IH}) is indeterminate.

Fast Page Mode Cycle (Read, Write, Read-Write and Read-Modify-Write Cycles) (Note 23)

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t _{PC}	Fast page mode read/write cycle time	40		45		50		ns
t _{PRWC}	Fast page mode read write/read modify write cycle time	75		95		100		ns
t _{RAS}	RAS low pulse width for read write cycle (Note 24)	100	100000	115	100000	135	100000	ns
t _{CP}	CAS high pulse width (Note 25)	10	15	10	20	10	20	ns
t _{CPPH}	RAS hold time after CAS precharge	35		40		45		ns
t _{CPWD}	Delay time, CAS hold time after W low (Note 22)	35		40		45		ns

Note 23 All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle
 Note 24 t_{RAS(min)} is specified as two cycles of CAS input are performed
 Note 25 t_{CP(max)} is specified as a reference point only

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CAS before RAS Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t _{CSR}	CAS setup time before RAS low	10		10		10		ns
t _{CHR}	CAS hold time after RAS low	10		15		15		ns
t _{RSR}	Read setup time before RAS low	10		10		10		ns
t _{RHR}	Read hold time after RAS low	10		15		15		ns
t _{CAS}	CAS low pulse width	25		30		30		ns

Note 26 Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode

TEST MODE SPECIFICATION (Note 27)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I _{CC1(AV)}	Average supply current from V _{CC} operating (Note 3, 4)	M5M44400A-6, -6L	RAS, CAS cycling t _{RC} =t _{WC} =min output open			115	mA
		M5M44400A-7, -7L				100	
		M5M44400A-8, -8L				85	
I _{CC3(AV)}	Average supply current from V _{CC} refreshing (Note 3)	M5M44400A-6, -6L	RAS cycling, CAS = V _{IH} t _{RC} =min output open			115	mA
		M5M44400A-7, -7L				100	
		M5M44400A-8, -8L				85	
I _{CC4(AV)}	Average supply current from V _{CC} Fast-Page-Mode (Note 3, 4)	M5M44400A-6, -6L	RAS = V _{IL} , CAS cycling t _{PC} =min output open			115	mA
		M5M44400A-7, -7L				100	
		M5M44400A-8, -8L				85	
I _{CC6(AV)}	Average supply current from V _{CC} CAS before RAS refresh mode (Note 3)	M5M44400A-6, -6L	CAS before RAS refresh cycling t _{RC} =min output open			100	mA
		M5M44400A-7, -7L				85	
		M5M44400A-8, -8L				75	

Note 27 All previously specified electrical characteristics, switching characteristics and timing requirements are applicable to that of test mode

SWITCHING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Notes 5, 12, 13)

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t _{OAC}	Access time from CAS (Note 6, 7)		20		25		25	ns
t _{RAC}	Access time from RAS (Note 6, 8)		65		75		85	ns
t _{AA}	Column address access time (Note 6, 9)		35		40		45	ns
t _{OPA}	Access time from CAS precharge (Note 6, 10)		40		45		50	ns
t _{OEA}	Access time from OE (Note 6)		20		25		25	ns

M5M44400AWJ,J,L,TP,RT-6,-7,-8,-6L,-7L,-8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Notes 12, 13)

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t _{RC}	Read cycle time	125		145		165		ns
t _{RAS}	RAS low pulse width	65	10000	75	10000	85	10000	ns
t _{CAS}	CAS low pulse width	20	10000	25	10000	25	10000	ns
t _{CSH}	CAS hold time after RAS low	65		75		85		ns
t _{RSH}	RAS hold time after CAS low	20		25		25		ns
t _{RAL}	Column address to RAS hold time	35		40		45		ns
t _{OCH}	CAS hold time after OE low	20		25		25		ns
t _{ORH}	RAS hold time after OE low	20		25		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t _{RWC}	Read write/read modify write cycle time (Note 21)	165		190		210		ns
t _{RAS}	RAS low pulse width	100	10000	120	10000	130	10000	ns
t _{CAS}	CAS low pulse width	55	10000	70	10000	70	10000	ns
t _{CSH}	CAS hold time after RAS low	100		120		130		ns
t _{RSH}	RAS hold time after CAS low	55		70		70		ns
t _{OWD}	Delay time, CAS low to W low (Note 22)	40		45		45		ns
t _{RWD}	Delay time, RAS low to W low (Note 22)	85		95		105		ns
t _{AWD}	Delay time address to W low (Note 22)	55		60		65		ns

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 22)

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t _{PC}	Fast page mode read/write cycle time	45		50		55		ns
t _{PRWC}	Fast page mode read write/read modify write cycle time	80		100		105		ns
t _{RAS}	RAS low pulse width for read write cycle (Note 24)	110	100000	125	100000	145	100000	ns
t _{CPRH}	RAS hold time after CAS precharge	40		45		50		ns
t _{CPWD}	Delay time, CAS precharge to W low (Note 22)	40		45		50		ns

Test Mode Set Cycle

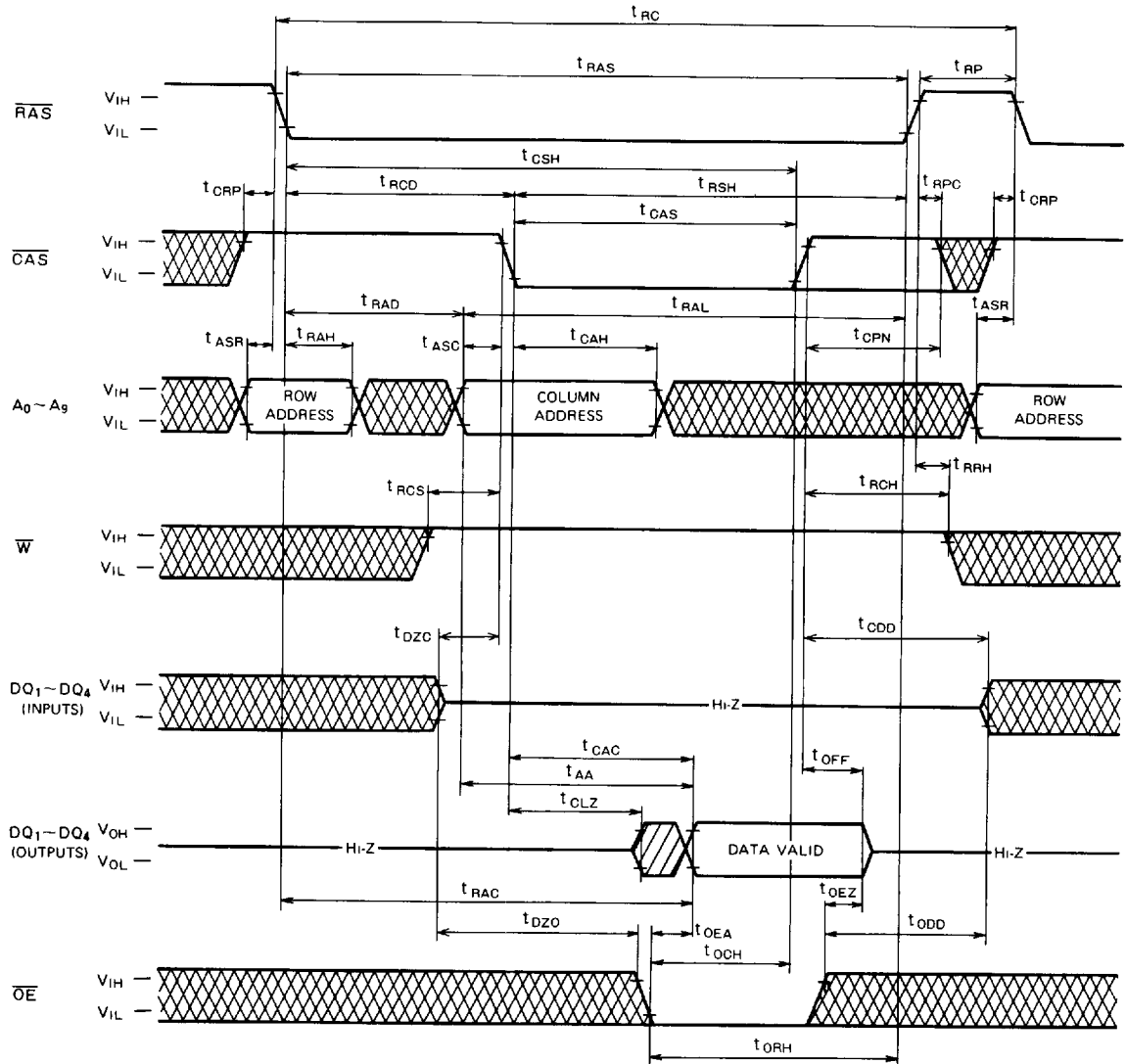
Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t _{WSR}	Write setup time before RAS low	10		10		10		ns
t _{WHR}	Write hold time after RAS low	10		15		15		ns



M5M4440AWJ, J, L, TP, RT-6, -7, -8, -6L, -7L, -8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

Timing Diagrams (Note 28)

Read Cycle

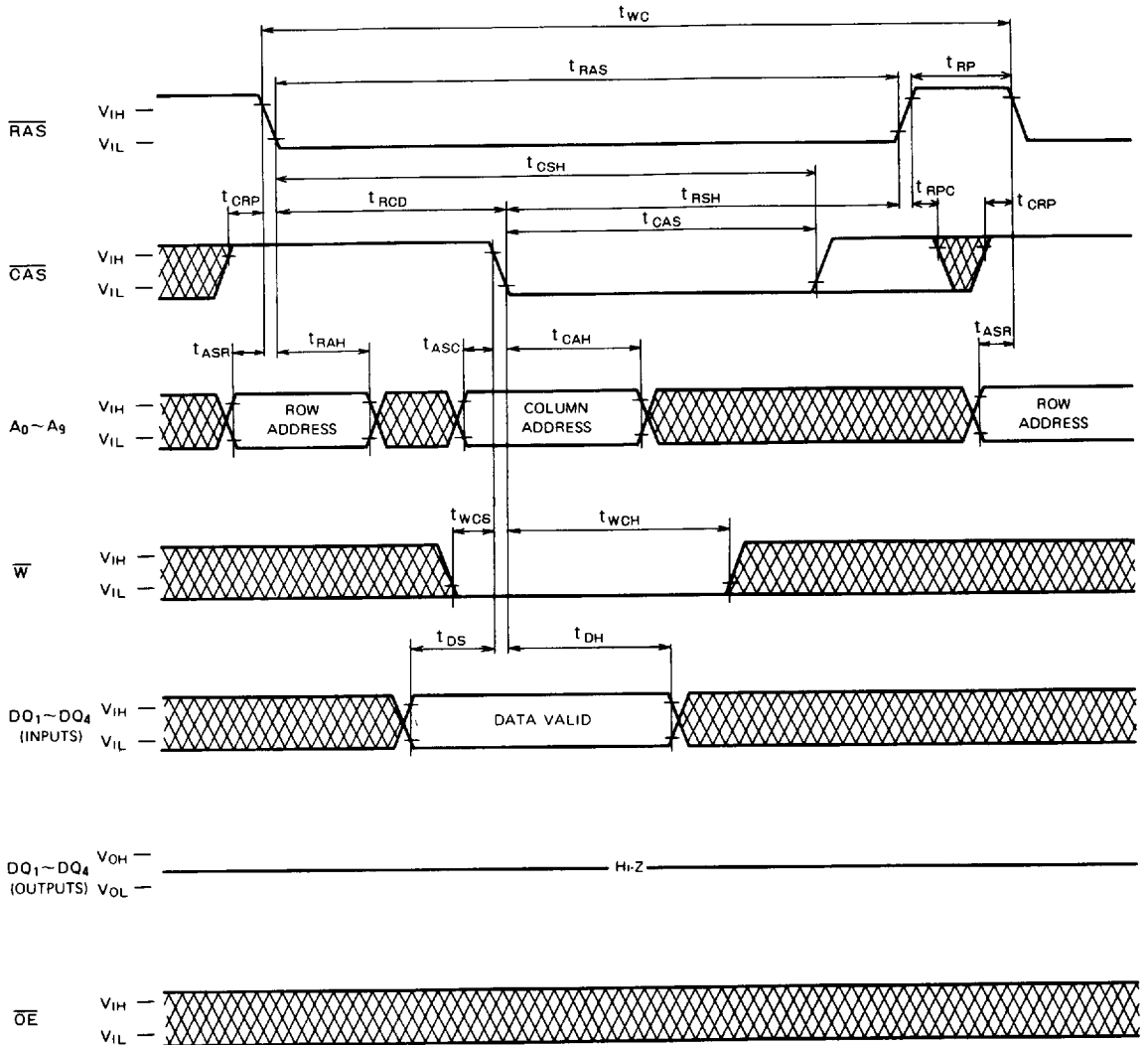


Note 28  Indicates the don't care input
 $V_{IH(min)} \leq V_{IN} \leq V_{IH(max)}$ or $V_{IL(min)} \leq V_{IN} \leq V_{IL(max)}$
 Indicates the invalid output

M5M44400AWJ, J, L, TP, RT-6, -7, -8, -6L, -7L, -8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

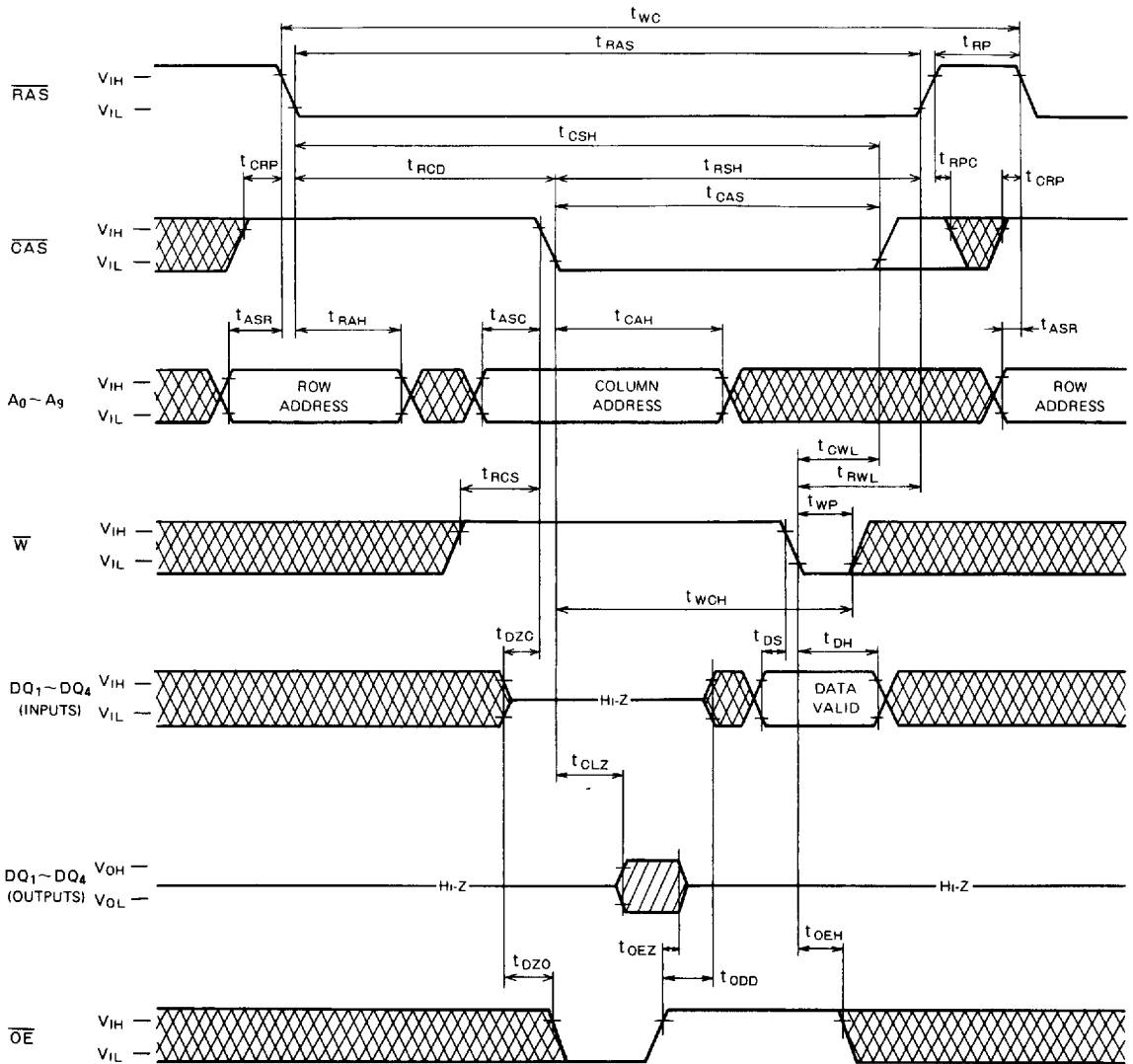
Write Cycle (Early write)



M5M44400AWJ, J, L, TP, RT-6, -7, -8, -6L, -7L, -8L

FAST PAGE MODE 4194304-BIT (1048576 WORD BY 4-BIT) DYNAMIC RAM

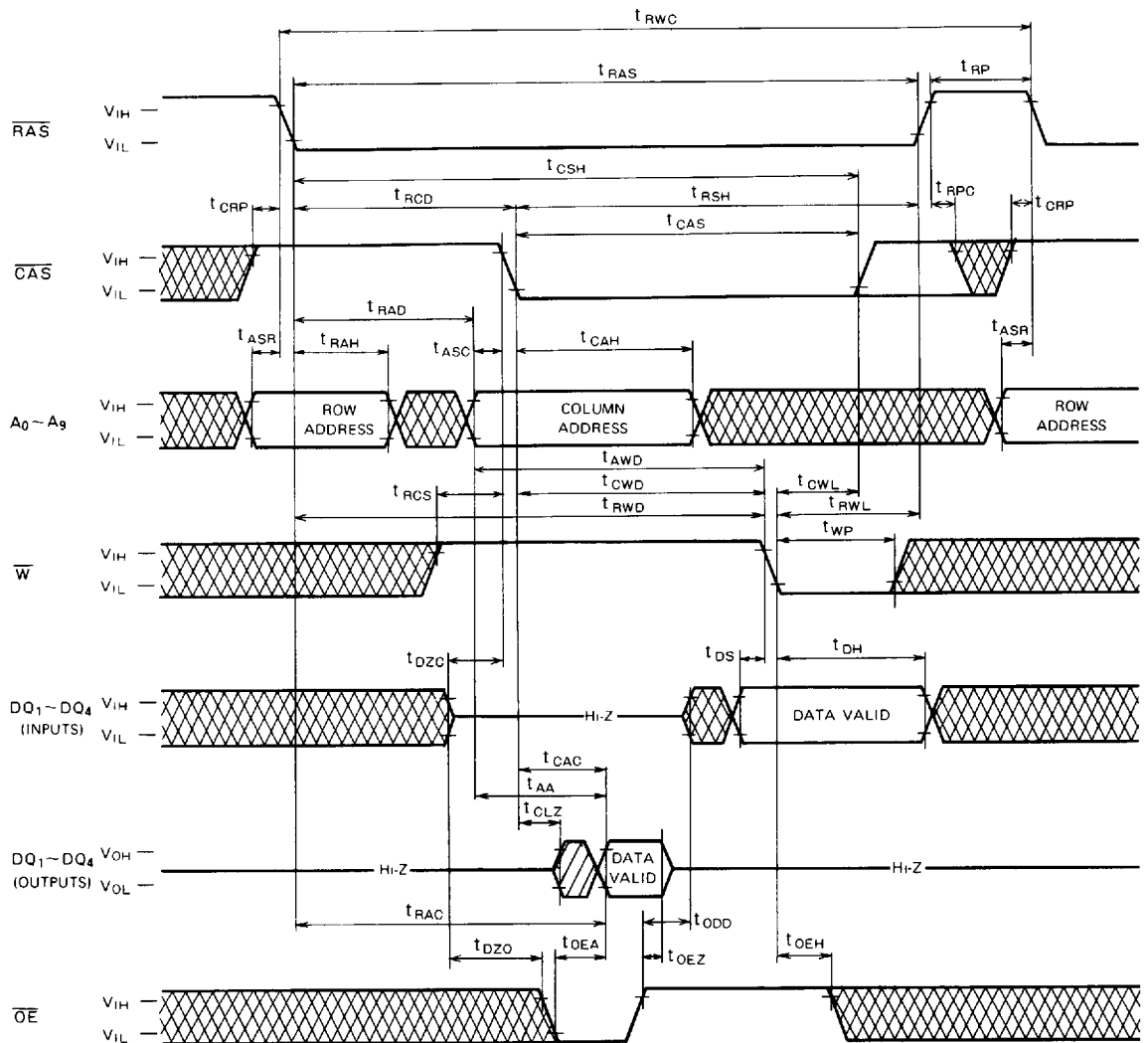
Write Cycle (Delayed Write)



M5M44400AWJ, J, L, TP, RT-6, -7, -8, -6L, -7L, -8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

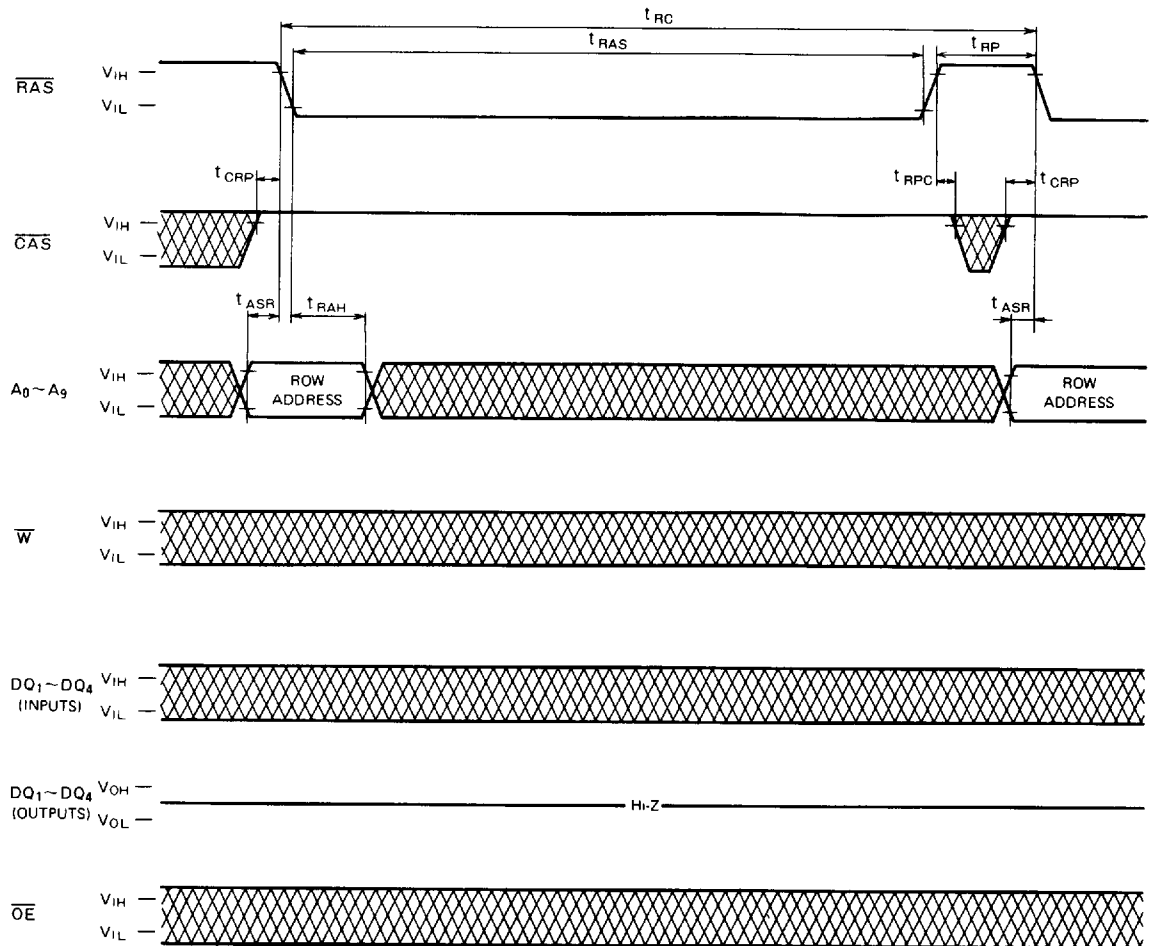
Read-Write, Read-Modify-Write Cycle



M5M44400AWJ, J, L, TP, RT-6, -7, -8, -6L, -7L, -8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

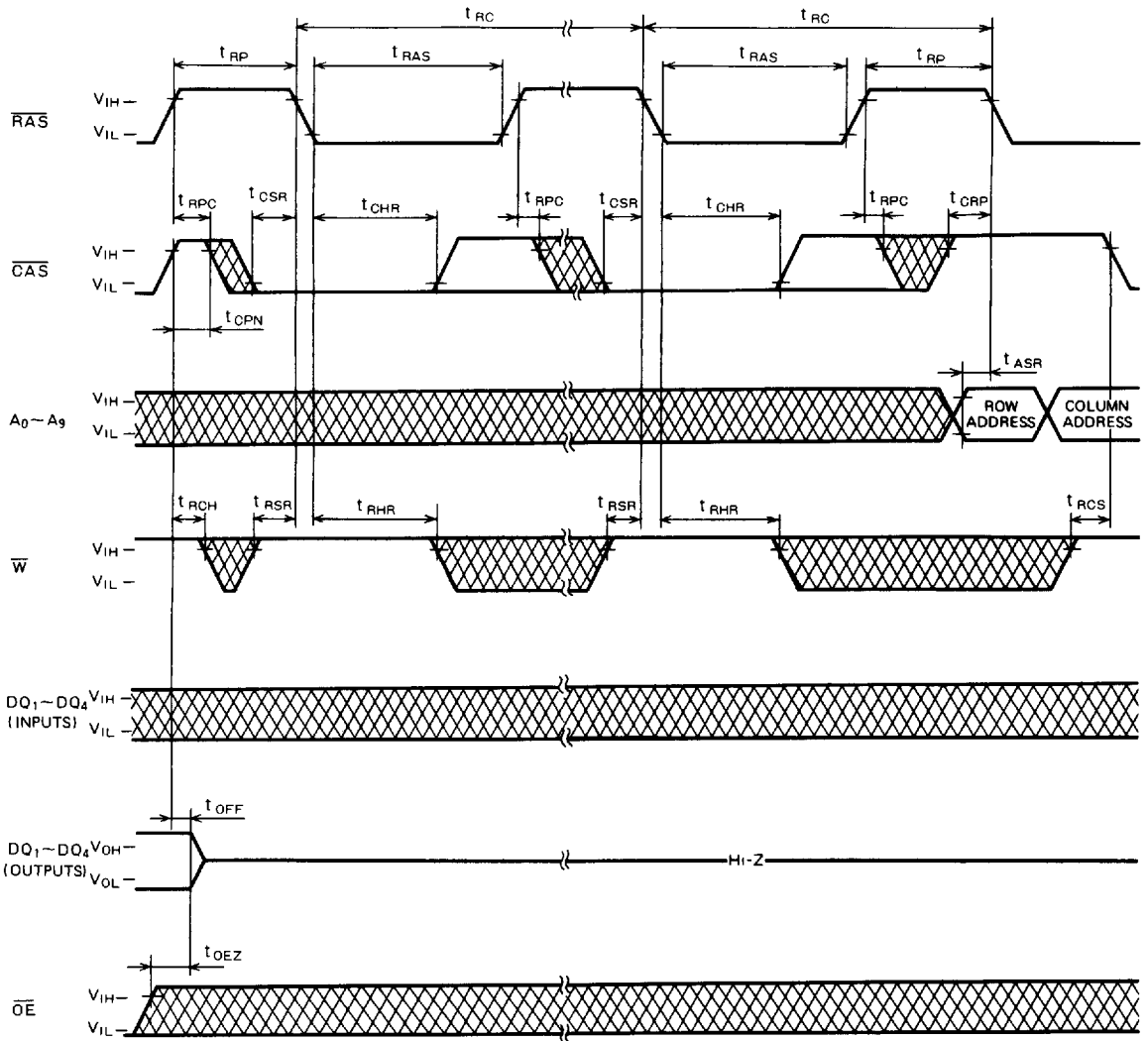
RAS-only Refresh Cycle



MSM44400AWJ, J, L, TP, RT-6, -7, -8, -6L, -7L, -8L

FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

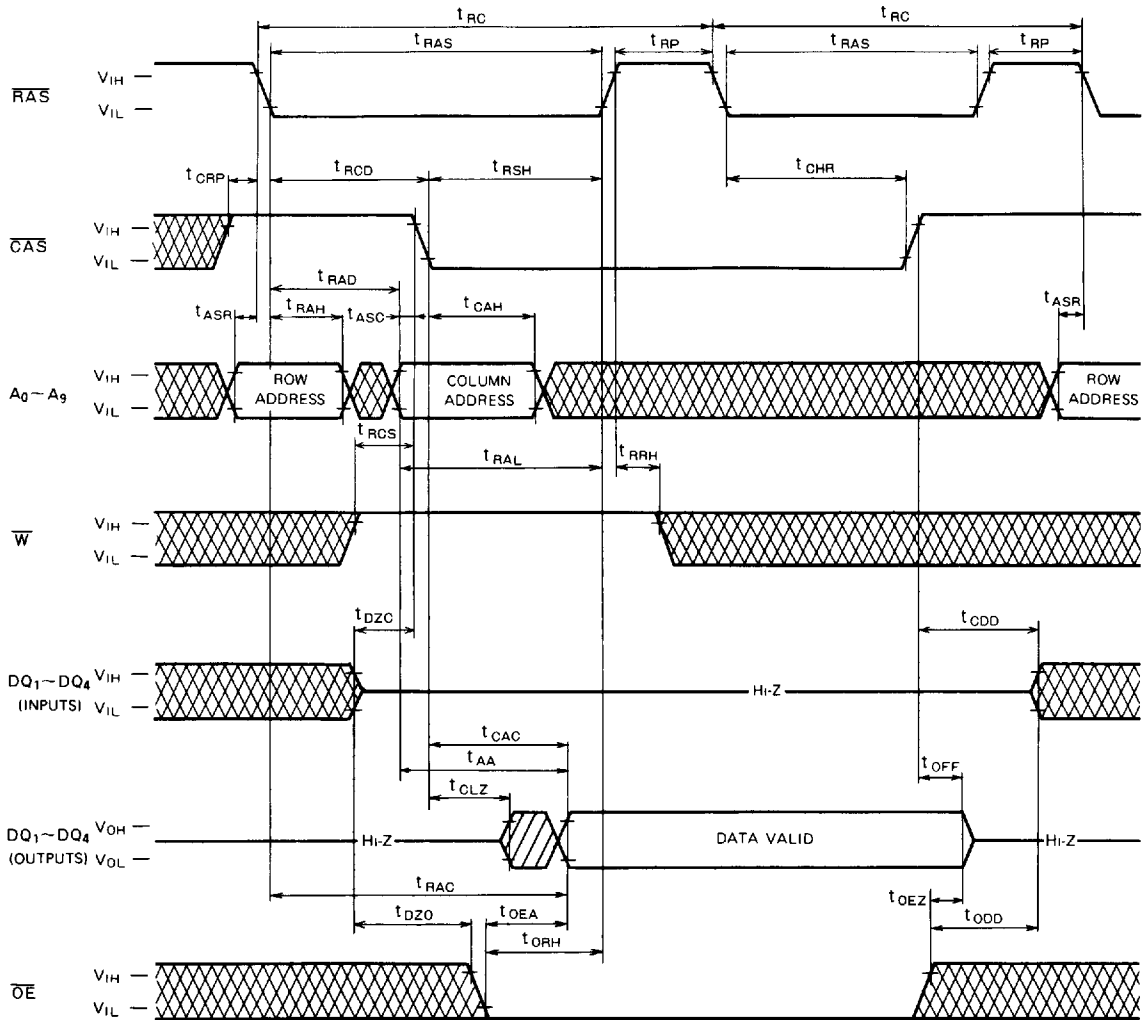
CAS before RAS Refresh Cycle



M5M44400AWJ, J, L, TP, RT-6, -7, -8, -6L, -7L, -8L

FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 29)

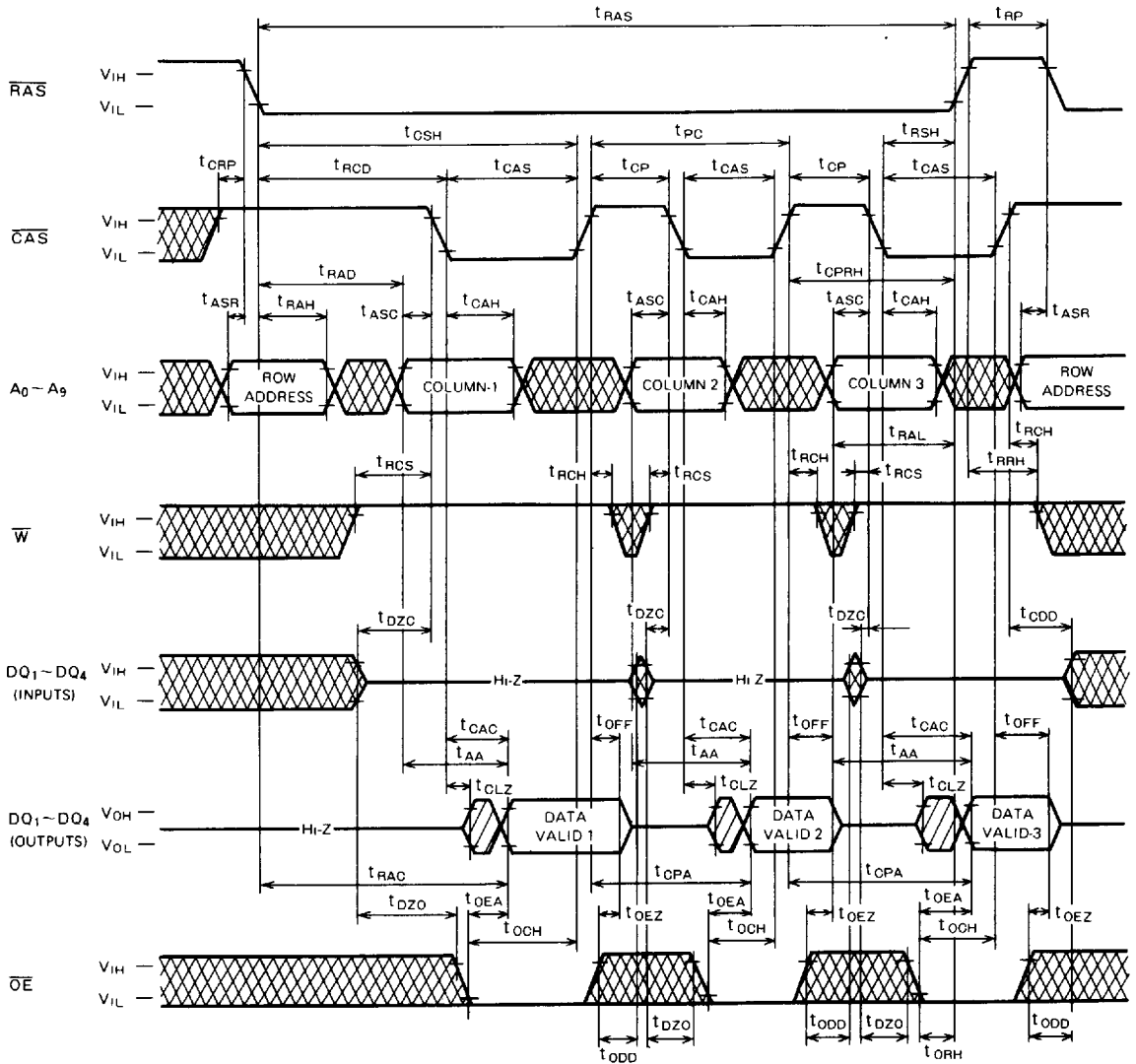


Note 29 Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above

M5M4400AWJ,J,L,TP,RT-6,-7,-8,-6L,-7L,-8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

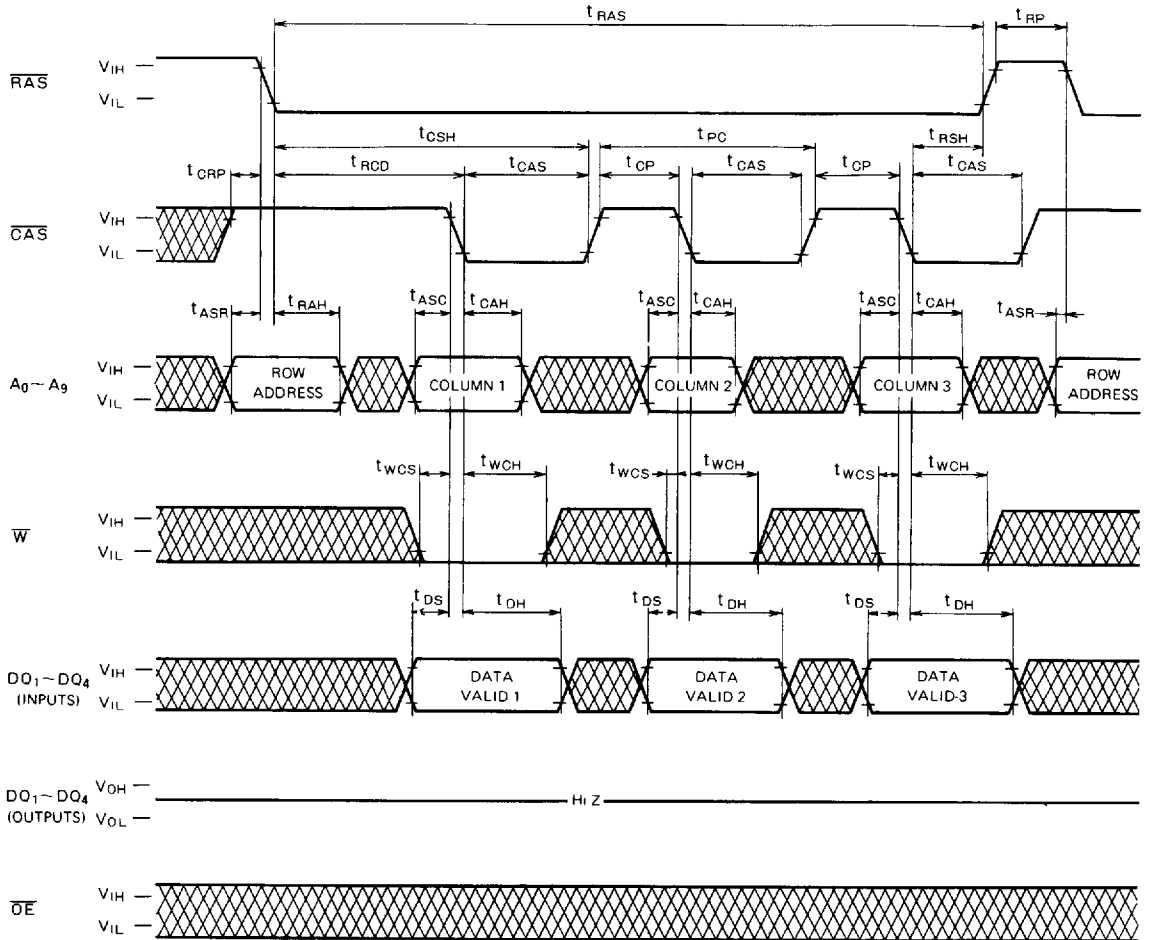
Fast Page Mode Read Cycle



MSM44400AWJ, J, L, TP, RT-6, -7, -8, -6L, -7L, -8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

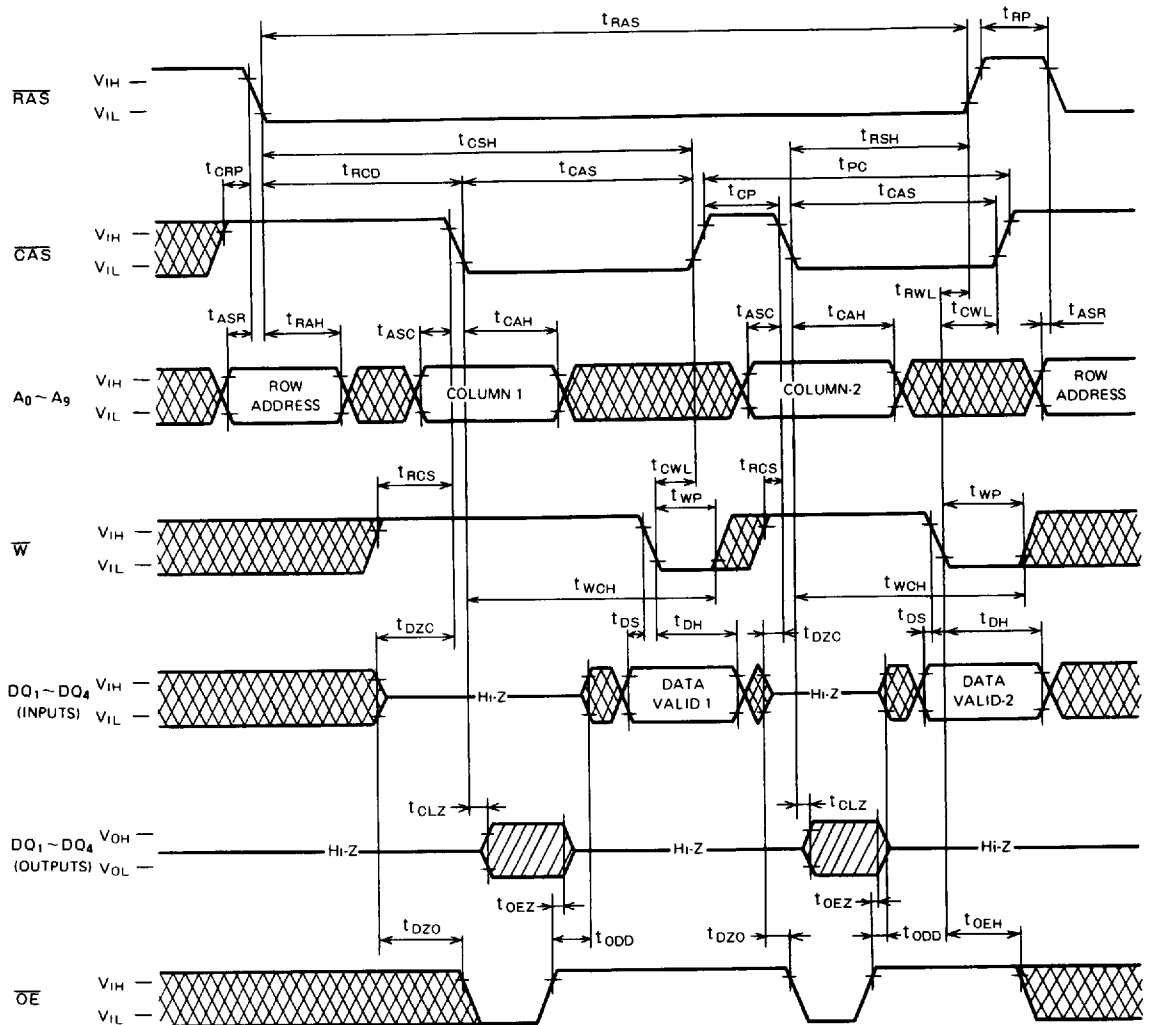
Fast Page Mode Write Cycle (Early Write)



M5M44400AWJ,J,L,TP,RT-6,-7,-8,-6L,-7L,-8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

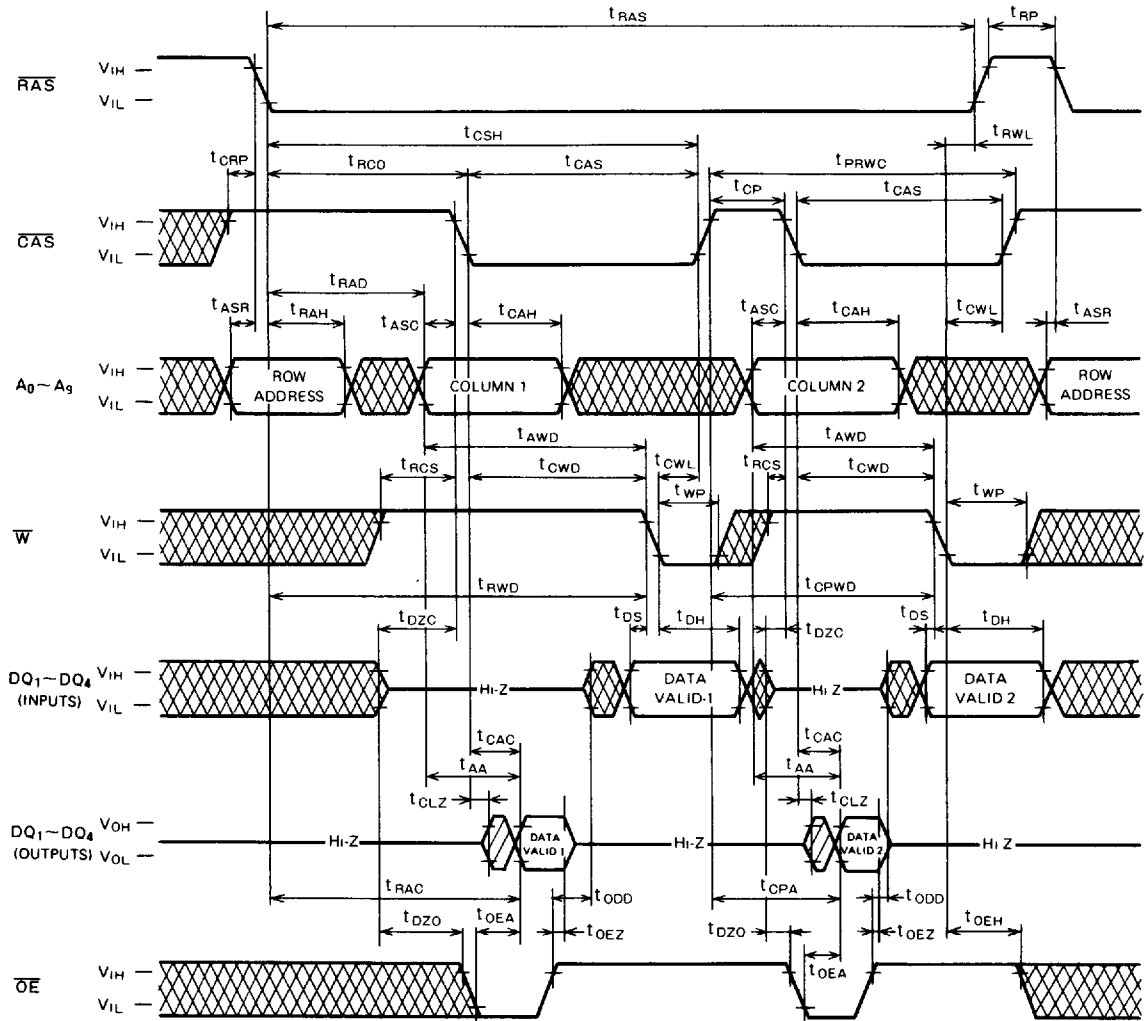
Fast Page Mode Write Cycle (Delayed Write)



M5M44400AWJ, J, L, TP, RT-6, -7, -8, -6L, -7L, -8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

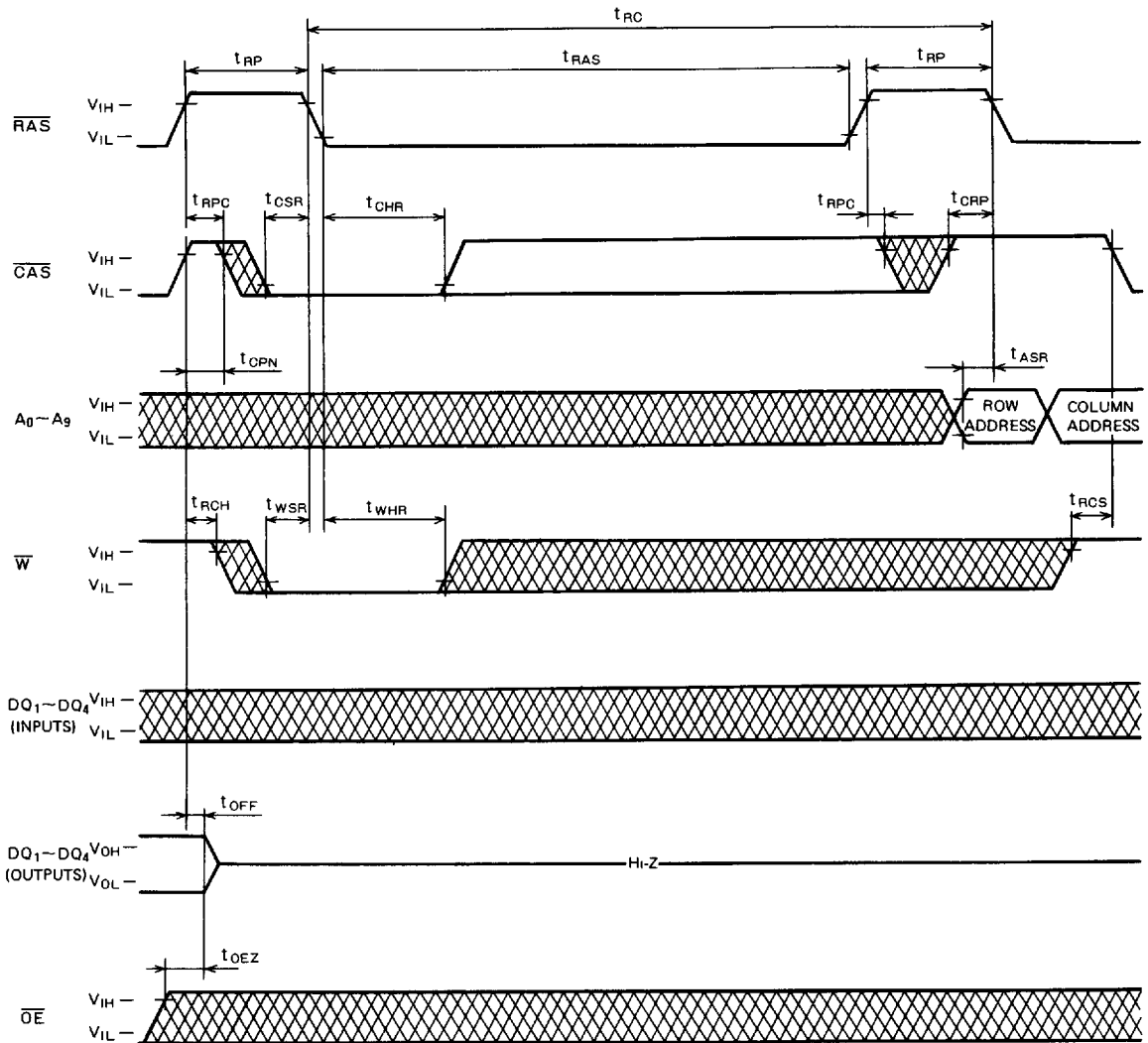
Fast Page Mode Read-Write, Read-Modify-Write Cycle



M5M44400AWJ,J,L,TP,RT-6,-7,-8,-6L,-7L,-8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

Test Mode Set Cycle (Note 30)



Note 30 This cycle is also available for the initialization cycle, but in this case device enters test mode. The test mode function is initiated with a \overline{W} and \overline{CAS} before \overline{RAS} cycle (WCBR cycle) as specified above timing diagram. The test mode function is terminated by either a \overline{CAS} before \overline{RAS} (CBR) refresh or a \overline{RAS} only refresh cycle. During the test mode, the device is internally organized as 4 bits wide (256 kilobytes deep) for each DQ (input/output) port. No addressing of A_0, A_1 (column only) is required. During a write cycle, data on the each DQ (input) pin is written in parallel into all 4 bits for each DQ port and can be written independently for each DQ port. During a read cycle, the each DQ (output) pin indicates independently a HIGH state if all 4 bits are equal, and a LOW state if any bits differ. During the test mode operation, a WCBR cycle is used to perform refresh.